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# Boosting RF / Analog Performance: Junctionless MOSFET with SiGe Pocket Doping

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*Abstract— This study explores the efficiency of SiGe pocket doping within the channel of silicon-based junctionless MOSFETs for controlling leakage current while enhancing radiofrequency (RF) performance. Junctionless MOSFETs have garnered attention for their simplified fabrication process and reduced short-channel effects compared to traditional transistors. However, managing leakage current remains crucial, especially in high-frequency analog circuits with stringent performance requirements. This research investigates its dual role in mitigating leakage current and boosting RF characteristics by strategically incorporating SiGe pocket doping. Through extensive silvaco TCAD simulations, we explore the impact of SiGe pocket doping on analog and RF performance. The proposed device yields a 5.093×10-13A off-current, 1.5 mA on-current, 0.41 threshold voltage, switching speed is 10<sup>9</sup> , transconductance is 38.4 mS, and cut-off frequency of 468.44 GHz. The findings reveal that SiGe pocket doping effectively confines carriers, thereby minimizing leakage paths and improving RF performance parameters. This research paves the way for future exploration of material combinations and fabrication techniques to unlock the full potential of double gate junctionless MOSFETs with SiGe pocket doping and differentially doped channels. These findings highlight the possibility of using SiGe pocket doping as a practical method to improve the performance and dependability of junctionless MOSFETs in analog radio applications.*

*Keywords: junctionless, SiGe, pocket doping, cut-off frequency.*

#### **I. INTRODUCTION**

Semiconductor device sizes are constantly becoming smaller and are already approaching the nanoscale necessity for high-performance semiconductors has motivated research and development in this sector, low-power electronic devices [1]. A semiconductor device called a metal-oxidesemiconductor field-effect transistor (MOSFET) is utilized in a variety of applications, including analog and radio frequency (RF) applications, to handle high-power radio frequency signals from appliances like televisions, radio transmitters, and amplifiers [2]. Applying different materials with different doping profiles in the channel area of a Double Gate Junctionless MOSFET (DG-JL-MOSFET) has demonstrated encouraging outcomes. The application of several materials, such as In0.53Ga0.47As nanotubes, Si nanotubes, and SiGe layers, has been studied [3]. Optimizing doping concentrations for certain goals, such as matching threshold voltage or obtaining similar ON current, has been shown to result in notable improvements in drain current and subthreshold properties. In addition, improved subthreshold slope, ON/OFF current ratios, and RF Performance have been attained with the use of Dual Insulator architectures and reduced doping concentrations in certain layers [4]. These developments demonstrate how material and doping engineering in DG-JL-MOSFET channel regions may be used to enhance device performance for upcoming RF and low-power applications. Compared to conventional devices, this unique transistor shape has several benefits, including better control over channel doping, lower leakage current, and higher device performance [5].

A novel approach utilizes the benefits of DG-MOSFET. This work involves doping silicon-based junctionless MOSFETs' channels with SiGe material as SiGe pocket doping. This material allows for the independent doping of individual layers with different impurity concentrations. Doping adjusts the material's conductivity and offers advantages of its own. This makes it possible to regulate the electrical activity of the whole channel region much more precisely [6, 7]. In this case, the doping concentrations in the source and drain regions differ, but the material used in both is silicon (Si). Putting titanium dioxide (TiO<sub>2</sub>) in the channel area of a DG-JFET as a high-k dielectric material uses less energy more efficiently than  $SiO<sub>2</sub>$  because it has reduced leakage current, especially at low gate voltages.

#### **II. DEVICE CONFIGURATION AND SPECIFICATION**

This transistor design utilizes a double-gate junctionless MOSFET (DG-JFET) with a very thin silicon film and a specific gate oxide material. The entire structure is flat, and has the dimensions as the gate length (Lg) of 22 nanometers (nm) is very small, indicating a highly miniaturized transistor. A very thin layer of silicon makes up the transistor's channel area, with a silicon film thickness (Tsi) of 10 nanometers (nm). HfO2 and TiO2 are the material used as Gate oxide (Tox). TiO2 works as the insulator between the gate and the channel, chosen for its beneficial properties. The



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same way HfO2 offers potential advantages for JFETs due to its high permittivity and potentially lower leakage current. This technique modifies a junctionless MOSFET's channel area by applying distinct material as pocket doping. As a result, a structure is designed, which has many potential benefits over a conventional, single-material silicon channel. SiGe is the material employed in this method.



Fig.1 (a) This is a conventional a double gate junctionless.





SiGe, or silicon-germanium, is an alloy composed of germanium (Ge) and silicon (Si). The mobility of electrons and holes (charge carriers) within silicon can be improved by mixing with germanium. This results in devices being faster and more effective. SiGe has unique benefits, such as compatibility with current silicon CMOS production techniques. This lowers research and manufacturing costs by making it easier to integrate SiGe into current silicon technology. An effective method for attaining better threshold voltage control, increased mobility, and perhaps steeper subthreshold swing in junctionless MOSFETs is SiGe pocket doping. In a double-gate junctionless MOSFET (DG-JFET) with SiGe pocket doping, using a gate electrode with a work function of 4.85 eV offers potential benefits. The higher work function can help counteract the potential screening effects arising from the higher doping concentration. A higher permittivity, makes it possible to obtain the same gate capacitance with a thinner oxide layer. This can help reduce the number of transistors used and possibly boost performance. For a given capacitance, HfO2 provides the thinnest layer that is achievable. Broader bandgaps are typically associated with increased device dependability and better resistance to leakage current. Table 1 shows all the parameters that are utilized in this work.







**Fig.1 (d)** is a calibrated graph of conventional and proposed devices.





**Table 1-** All of the values utilized in the proposed device are listed in this table 1.



#### **III. RESULT AND DISCUSSION**

The study demonstrates that in contrast to a device with a different oxide materials and a work function identical to the proposed device, using SiGe pocket doping in the channel region can result in a reduction in capacitance and a decrease in a device's off current.

The DGJLMOSET's Id/Vgs characteristics are shown in fig 2. The DG-JLMOSFET, SiGe pocket doping with TiO2 has a low on-current with respect to the DG-JLMOSFET with HfO2, according to the curve. DG-JLMOSFET with TiO2 has lowest off-current. A very low off current translates to minimal leakage and improved power efficiency. This is especially important for battery-powered devices.





**Fig.3** is a  $g_m$  (transconductance) plot that shows that SiGe pocket JL with TiO2 has a higher gm.

SiGe can provide better electron mobility than pure silicon. Mobility measures how readily electrons pass through a material, affecting both gm and current flow. A greater mobility corresponds to a more efficient electron flow, which raises the JLMOS's gm which is shown in fig.3. For transistors used in analog and radio frequency circuits, high transconductance is a desired property. Transconductance is a measure of how well the gate voltage affects the drain current; a device that responds more readily to the gate voltage would have a higher drain current (because of a more conductive channel). A higher transconductance value results from this, because interface trap density and gate control are well-balanced, HfO2 often has strong transconductance.TiO2 has a higher dielectric constant  $(κ)$ , which makes the oxide layer thinner. This may potentially result in increased transconductance and a stronger gate electric field. The equation to evaluate  $g_m$  is given in equation (1).





**Fig.4** represents a plot of the intrinsic capacitance of the three devices.



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In JFETs, the entire body acts as the channel, and Cgd reflects the ability of the gate to modulate the mobile charge carriers within it. JFETs as shown in fig.4 generally exhibit higher intrinsic capacitance compared to conventional MOSFETs due to the absence of the depletion region. A balance between gate control and high-frequency performance is provided by DG-JLMOSFET with TiO2.Reasonable gate control is offered for effective switching and gain. Due to the higher κ, a thinner  $TiO2$  layer can achieve the same capacitance as a thicker HfO2 layer, resulting in a potentially lower Cgd.



Fig.5 shows a plot of cut-off frequencies of three devices.

A key factor influencing cut-off frequencies is the transconductance (gm). As discussed earlier, g<sub>m</sub> reflects how efficiently the MOSFET converts a change in gate voltage into a change in drain current. A higher gm typically leads to a higher  $f_t$  in fig.5. While TiO2 has the potential for a higher fT due to a thinner achievable oxide and potentially higher gm, it requires addressing interface trap issues. HfO2 offers a more predictable and reliable performance with a moderate fT.While TiO2 offers the possibility of reduced leakage current and greater fT but with trade-offs, HfO2 is a better developed and dependable material. To calculate cut-off-frequency formula is given in equation.2.

$$
f_t = g_m/2\pi (C_{gs} + C_{gd})
$$
 (2)



**Fig.6** is a g<sub>d</sub> (output conductance) plot A lower gd translates to a more linear relationship between the drain current (Id) and the drain-to-source voltage (Vds) in the saturation region.

Lower gd translates to less additional current flow associated with changes in drain voltage shown in fig6. This leads to lower power dissipation within the JFET, reducing heating and improving overall circuit efficiency. The primary factor influencing gd is the doping concentration in the channel. Using a lower doping-level channel inherently leads to a lower gd.





The bandgap of the material narrows when silicon (Si) is combined with germanium (Ge) to form SiGe. In comparison to a pure silicon device, this enables the JMOSFET to achieve a lower threshold voltage (Vth).



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#### **IV. CONCLUSION**

Compared to traditional silicon channels, SiGe doping offers several advantages. It allows for precise control over the threshold voltage and enables the use of a wider bandgap material, potentially leading to a higher on-current. Additionally, SiGe pocket doping enhances carrier mobility, resulting in a significant increase in transconductance, a key parameter for signal amplification. Fig.1 (b) is an optimistic device. Furthermore, the combination of these factors contributes to a higher cut-off frequency, extending the device's operational range into the RF regime. Table.2 shows all values off different parameters that are the results of devices. These improvements make SiGe pocket doping a promising approach for developing high-performance DG-JFETs suitable for RF and analog applications.

#### **REFERENCES**

[1] D. Yadav, Madan Mohan Malaviya University of Technology, Ryūkyū Daigaku, Institute of Electrical and Electronics Engineers. Uttar Pradesh Section, and Institute of Electrical and Electronics Engineers, 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON) : proceeding : 2-4 November, 2018.

- [2] Sanjay, B. Prasad, and A. Vohra, "Performance evaluation of junctionless double surrounding gate In0.53Ga0.47As nanotube MOSFET using dual material gate engineering," Journal of Materials Science: Materials in Electronics, vol. 32, no. 7, pp. 9171–9182, Apr. 2021, doi: 10.1007/s10854-021- 05583-5.
- [3] Sanjay, B. Prasad, and A. Vohra, "Effect of 3 nm gate length scaling in junctionless double surrounding gate SiNT MOSFET by using triple material gate engineering," Microsystem Technologies, vol. 27, no. 10, pp. 3869–3874, Oct. 2021, doi: 10.1007/s00542-020-05182-0.
- [4] S. L. Tripathi, S. K. Sinha, and G. S. Patel, "Low-Power Efficient p+ Si0.7Ge0.3 Pocket Junctionless SGTFET with Varying Operating Conditions," J Electron Mater, vol. 49, no. 7, pp. 4291–4299, Jul. 2020, doi: 10.1007/s11664-020- 08145-3.
- [5] X. Cheng, "Overview of Recent Progress of Semiconductor Power Devices based on Wide Bandgap Materials," in IOP Conference Series: Materials Science and Engineering, Institute of Physics Publishing, Nov. 2018. doi: 10.1088/ 1757-899X/439/2/022033.
- [6] N. Mendiratta and S. L. Tripathi, "8nm n-channel and p-channel Dopingless Asymmetrical Junctionless DG-MOSFET: Low Power CMOS Based Digital and Memory Applications 18nm n-channel and p-channel Dopingless Asymmetrical Junctionless DG-MOSFET: Low Power CMOS based Digital and Memory Applications," 2021, doi: 10.21203/rs.3.rs-731654/v1.
- [7] J. Singh and R. K. Chauhan, "Synergic Effect of Misaligned Gate and Temperature on Hetero-Dielectric Double-Gate Junctionless Metal–Oxide-Semiconductor Field-Effect Transistors for High-Frequency Application," Physica Status Solidi (A) Applications and Materials Science, vol. 220, no. 23, Dec. 2023, doi: 10.1002/pssa.202300607.
	- [8] 2019 IEEE 5th International Conference for Convergence in Technology (I2CT). IEEE.
	- [9] International Institute of Information Technology (Pune, Institute of Electrical and Electronics Engineers. Pune Section, and Institute of Electrical and Electronics Engineers, International Conference on Automatic Control & Dynamic Optimization Techniques (ICACDOT 2016) : 9th & 10th September 2016.
	- [10] N. Mendiratta, S. L. Tripathi, and S. Chander, "Analytical Model of Dopingless Asymmetrical Junctionless Double Gate MOSFET," Silicon, vol. 14, no. 16, pp. 10765–10774, Nov. 2022, doi: 10.1007/s12633-022-01819-z.